

REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-18 are pending. Claims 10-18 have been added to secure an appropriate scope of protection to which Applicants are believed entitled. Claim 1 has been amended to recite that the second intermediate bus directly couples the system bus interface device to the switching device. Support for the subject matter of amended claim 1 is believed to be found at least at page 4, lines 2-3 and FIG. 1.

New claim 11 recites a configurable I/O bus architecture comprising a system bus interface device, first and second I/O bus interface devices, a switching device arranged to be responsive to a steering signal, a first intermediate bus coupling I/O bandwidth of the first I/O bus interface device with I/O bandwidth of the system bus interface device, and a second intermediate bus coupling I/O bandwidth of the switching device with I/O bandwidth of the system bus interface device, wherein the switching device couples I/O bandwidth of the second intermediate bus to I/O bandwidth of either the first or second I/O bus interface device responsive to the steering signal which is neither disclosed nor suggested by the applied references, singly or in combination.

New claim 16 recites an I/O bus architecture comprising at least one first I/O bus interface device, at least one second I/O bus interface device, a switching device connected to the at least one first I/O bus interface device and the at least one second I/O bus interface device, and a system bus interface device connected to the at least one first I/O bus interface device and the switching device, wherein the switching device is arranged to connect the system bus interface device to one of the at least one first I/O bus interface device and the at least one second I/O bus interface device responsive to a steering signal which is neither disclosed nor suggested by the applied references, singly or in combination.

Support for the subject matter of claims 11 and 16 is believed to be found at least at pages 3-6 and FIG. 1.

Amended claim 1 is patentable over Ajanovic et al.

The rejection of claims 1-4 and 9 under 35 USC 102(b) as being anticipated by Ajanovic et al. (US Patent 5,859,988) is believed overcome in view of the foregoing amendments. Specifically, Ajanovic fails to disclose the first intermediate bus directly coupling the system bus interface device to the first I/O bus interface device. As stated by the Patent & Trademark Office (PTO), Ajanovic appears to describe "second intermediate bus that is directly connected to port A/c Data buffers in 306, that is directly connected to buffer manager 307, that is directly connected to switch device." Final Office Action at page 6, lines 5-7. Therefore, Ajanovic fails to disclose all elements of claim 1 and withdrawal of the rejection is respectfully requested.

Claims 5-8 are patentable over Ajanovic et al. in view of Alexander et al.

The rejection of claims 5-8 under 35 USC 103(a) as being unpatentable over Ajanovic in view of Alexander et al. (US Patent 6,510,529) is believed overcome in view of the foregoing amendments. Claims 5-8 depend, either directly or indirectly, from claim 1, include further limitations, and are patentable over Ajanovic in view of Alexander for at least the reasons advanced above with respect to claim 1. Withdrawal of the rejection is respectfully requested.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

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